FAIRCHILD
SEMICONDUCTOR®

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MM74HC574
3-STATE Octal D-Type Edge-Triggered Flip-Flop

General Description

The MM74HC574 high speed octal D-type flip-flops utilize advanced silicon-gate P-well CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

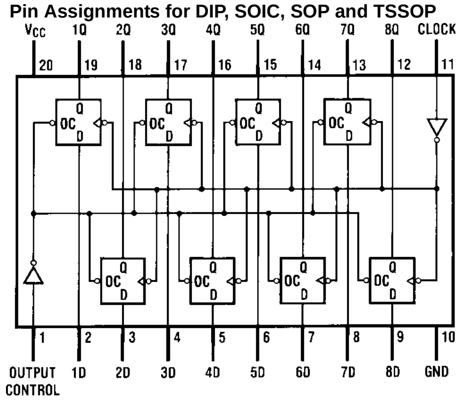
Ordering Code:

Order Number	Package Number	Package Description
MM74HC574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC574N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Truth Table

Output Control	Clock	Data	Output
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level
L = LOW Level
X = Don't Care
$\uparrow$ = Transition from LOW-to-HIGH
Z = High Impedance State
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	
			6.0V		4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	
			6.0V		1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	
			6.0V	6.0	5.9	5.9	5.9	
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	
			6.0V	0	0.1	0.1	0.1	
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum 3-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0V		±0.5	±5.0	±10	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA	6.0V		8.0	80	160	µA
ΔI_{CC}	Quiescent Supply Current per Input Pin	V_{CC} = 5.5V	OE	1.0	1.5	1.8	2.0	mA
		V_{IN} = 2.4V	CLK	0.6	0.8	1.0	1.1	
		or 0.4V (Note 4)	DATA	0.4	0.5	0.6	0.7	

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		60	33	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L = 45$ pF	17	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ $C_L = 45$ pF	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 5$ pF	14	25	ns
t_S	Minimum Setup Time, Data to Clock		10	12	ns
t_H	Minimum Hold Time, Clock to Data		−3	5	ns
t_W	Minimum Pulse Clock Width		8	15	ns

AC Electrical Characteristics

$V_{CC} = 2.0 - 6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

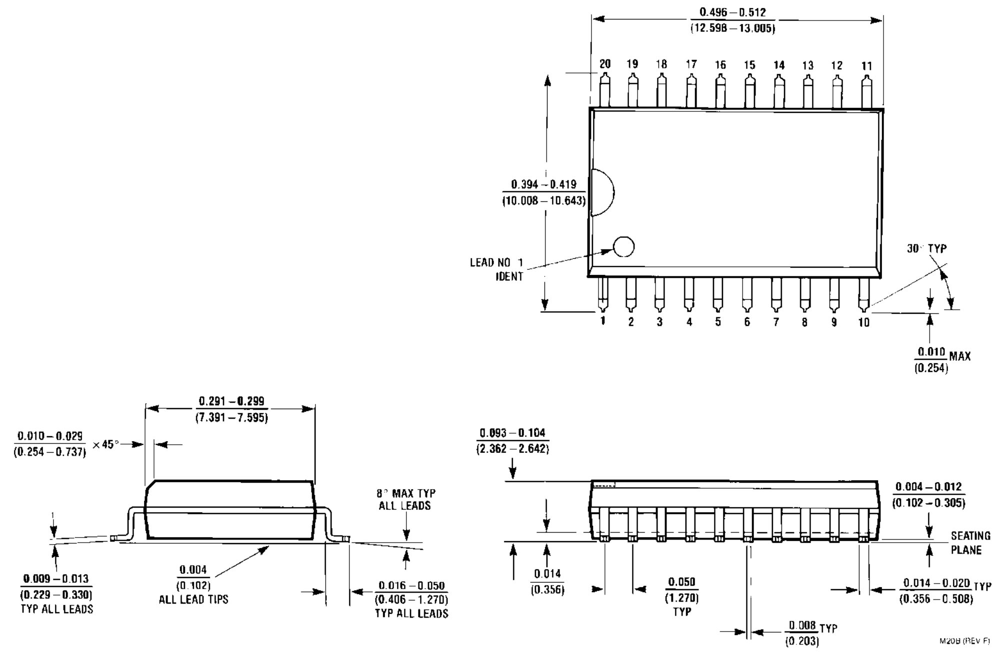
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L = 50$ pF	2.0V		33	28	23	MHz
			4.5V		30	24	20	
			6.0V		35	28	23	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L = 50$ pF	2.0V	18	30	38	45	ns
		$C_L = 150$ pF	2.0V	51	155	194	233	
		$C_L = 50$ pF	4.5V	13	23	29	35	ns
		$C_L = 150$ pF	4.5V	19	31	47	47	
		$C_L = 50$ pF	6.0V	12	20	25	30	ns
		$C_L = 150$ pF	6.0V	18	27	34	41	
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ						
		$C_L = 50$ pF	2.0V	22	30	38	45	ns
		$C_L = 150$ pF	2.0V	59	180	225	270	
		$C_L = 50$ pF	4.5V	14	28	35	42	ns
		$C_L = 150$ pF	4.5V	20	36	45	54	
		$C_L = 50$ pF	6.0V	12	24	30	36	ns
		$C_L = 150$ pF	6.0V	18	31	39	47	
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ	2.0V	15	30	38	45	ns
		$C_L = 50$ pF	4.5V	12	25	31	38	
			6.0V	10	21	27	32	
t_S	Minimum Setup Time Data to Clock		2.0V	6	12	15	18	ns
			4.5V		20	25	30	
			6.0V		17	21	25	
t_H	Minimum Hold Time Clock to Data		2.0V	−1	5	6	8	ns
			4.5V		0	0	0	
			6.0V		0	0	0	
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	2.0V	6	12	15	18	ns
			4.5V	7	12	15	18	
			6.0V	6	10	13	15	
t_W	Minimum Clock Pulse Width		2.0V	30	15	20	24	ns
			4.5V	9	16	20	24	
			6.0V	8	14	18	20	
t_r, t_f	Maximum Clock Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	
			6.0V		400	400	400	
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	$OC = V_{CC}$		5				pF
		$OC = GND$		58				
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

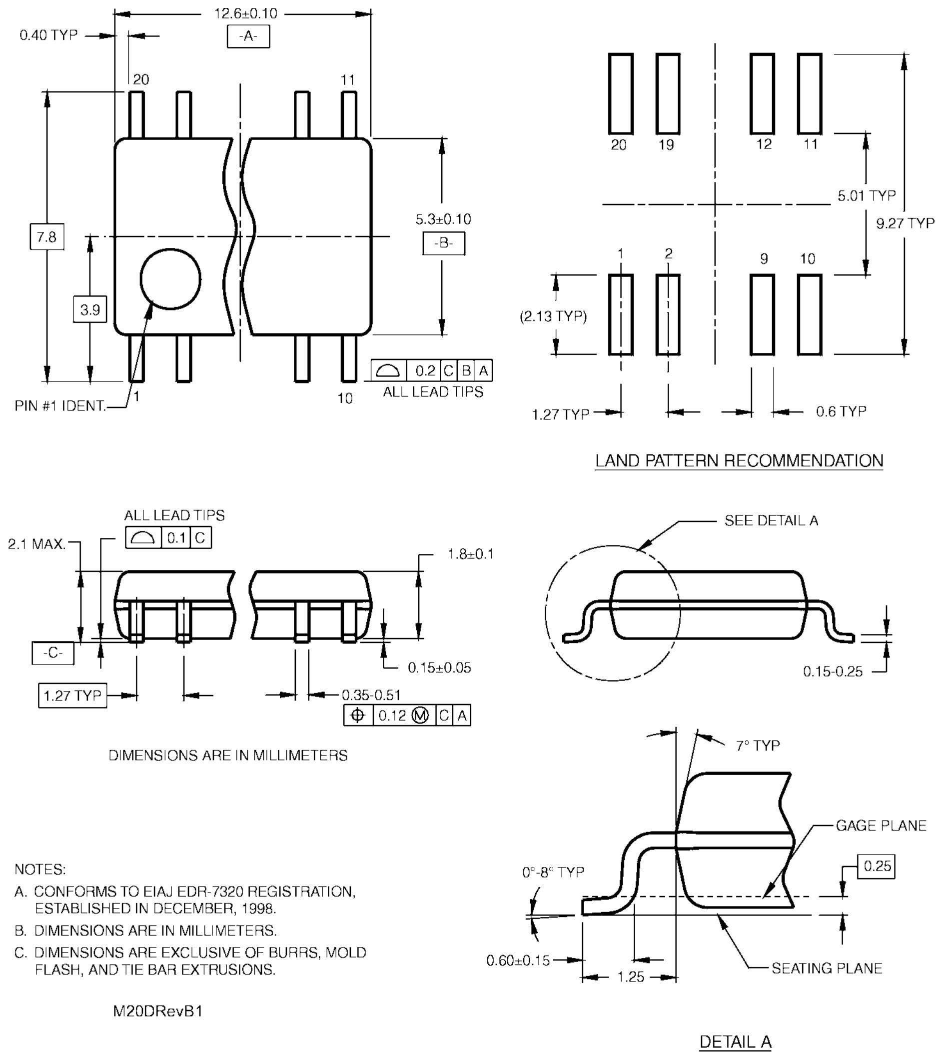
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted



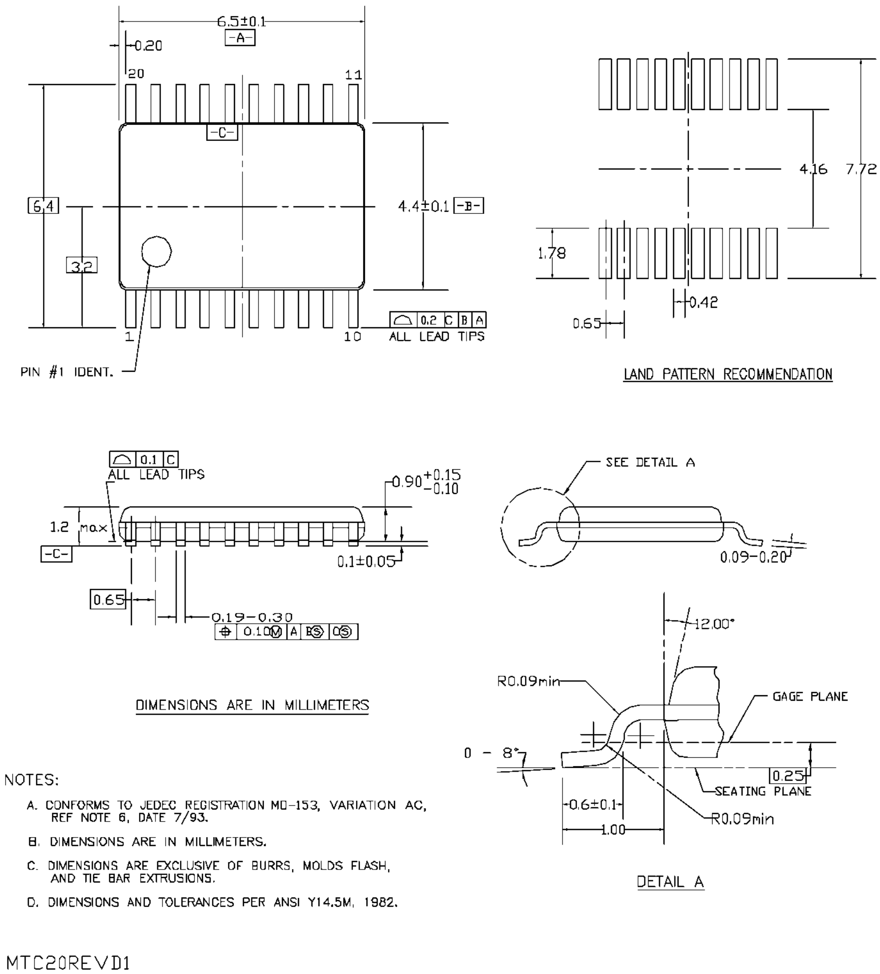
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



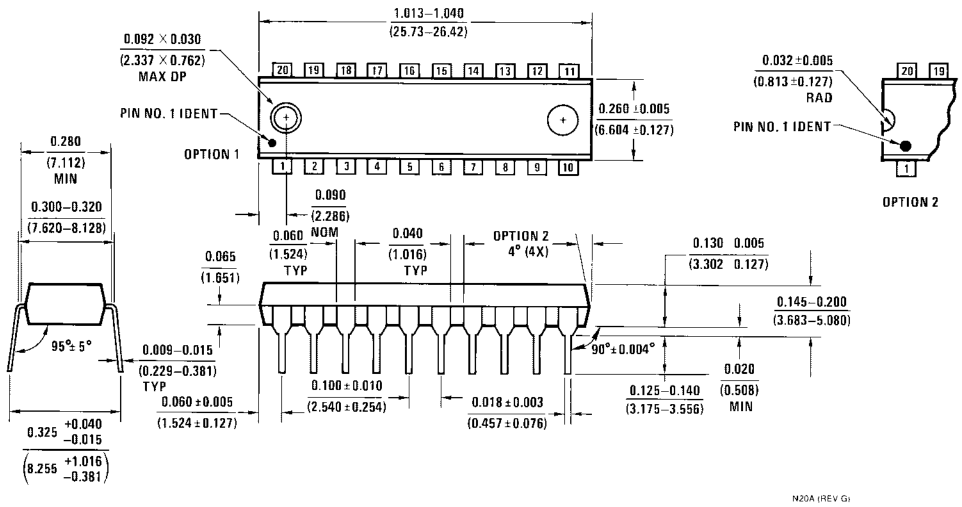
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A